IN THE CLAIMS

Please amend the claims as follows:

Claims 1-8 (Canceled).

Claim 9 (New): A logic circuit having a self-test function comprising:

a plurality of scanning flip-flop (F/F) circuits having at least a first-stage scanning F/F circuit, a second-stage scanning F/F circuit and a last-stage scanning F/F circuit, each having a clock input terminal, a scanning input terminal and a scanning output terminal, the scanning F/F circuits being connected to one another so that a scanning clock signal is input to the clock input terminal of each scanning F/F circuit and a signal output from the scanning output terminal of the first-stage scanning F/F circuit is supplied to the scanning input terminal of the second-stage scanning F/F circuit for sequential logical operations;

a feed-back signal line through which a signal from the scanning output terminal of the last-stage scanning F/F circuit is fed back;

at least one data selector to select either an external scanning signal or the signal fed back from the last-stage scanning F/F circuit, the selected signal being supplied to the scanning input terminal of the first-stage scanning F/F circuit;

at least one scanning controller to supply a control signal to the data selector so that the signal fed back from the last-stage scanning F/F circuit is supplied to the scanning input terminal of the first-stage F/F scanning circuit, thus controlling each scanning F/F circuit in an internal scanning mode;

an external scanning output terminal via which the signal fed back from the last-stage scanning F/F circuit is output from the logic circuit;

at least one clock selector to select either an external scanning clock signal or an internal scanning clock signal supplied from the scanning controller, the selected scanning clock signal being supplied to the clock input terminal of each scanning F/F circuit;

an external clock output terminal via which the selected scanning clock signal supplied to the clock input terminal of each scanning F/F circuit is output from the logic circuit;

a disable-signal input terminal via which a disable signal for externally activating each scanning F/F circuit is input to the scanning controller to set an external F/F-scanning mode; and

an enable output terminal via which an enable signal is output from the logic circuit, the enable signal indicating that the scanning F/F circuits are active in the sequential logical operations in the external F/F-scanning mode,

wherein the scanning controller supplies the enable signal as an internal stall signal to the scanning F/F circuits when the enable signal is output from the logic circuit via the enable output terminal, the internal stall signal inhibiting the scanning clock signal to be supplied to the scanning F/F circuits.

Claim 10 (New): The logic circuit according to claim 9, wherein the scanning controller supplies the control signal to the data selector based on a processor instruction of a pre-stored program.

Claim 11 (New): The logic circuit according to claim 10, wherein the processor instruction is a reduced instruction set computer instruction.

Claim 12 (New): The logic circuit according to claim 10, wherein the scanning F/F circuits are divided into a plurality of logic-circuit groups each including the data selector, the clock selector and the scanning controller.

Claim 13 (New): The logic circuit according to claim 9 further comprising a serial-to-parallel converter, connected to the external scanning clock output terminal, the external scanning output terminal and the enable output terminal, to convert serial data output from the external scanning output terminal to parallel data.

Claim 14 (New): The logic circuit according to claim 9, wherein, in response to an external rotate signal, the scanning controller advances an installed program by one cycle after one logical sequential logical operation of the scanning F/F circuits for another logical sequential operation, and in response to an external step signal, the scanning controller outputs data of the scanning F/F circuits from the logic circuit after one-cycle program advancement in response to the rotate signal and then brings the logic circuit to a halt.